

| L Number | Hits | Search Text  | DB                               | Time stamp          |
|----------|------|--|----------------------------------|---------------------|
| 9        | 1    | (gate adj electrode) and (drain adj electrode) and (source adj electrode) and (L adj G adj Philips) and hole and (semiconductor near2 (film or layer)) and passivation | USPAT;<br>US-PGPUB               | 2004/10/28<br>08:52 |
| 10       | 3    | (gate adj electrode) and (drain adj electrode) and (source adj electrode) and (L adj G adj Philips) and hole   | USPAT;<br>US-PGPUB               | 2004/10/28<br>08:53 |
| 11       | 0    | (gate adj electrode) and (drain adj electrode) and (source adj electrode) and (L adj G adj Philips) and hole   | EPO; JPO;<br>DERWENT;<br>IBM TDB | 2004/10/28<br>08:53 |
| 12       | 10   | (gate adj electrode) and (drain adj electrode) and (source adj electrode) and (taiwan) and hole  | USPAT;<br>US-PGPUB               | 2004/10/28<br>08:54 |
| 13       | 110  | (gate adj electrode) and (drain adj electrode) and (source adj electrode) and (TW or Hsinchu or taipei) and hole   | USPAT;<br>US-PGPUB               | 2004/10/28<br>08:55 |
| 14       | 68   | ((gate adj electrode) and (drain adj electrode) and (source adj electrode) and (TW or Hsinchu or taipei) and hole ) and @ad<20020711                                   | USPAT;<br>US-PGPUB               | 2004/10/28<br>08:55 |

| L Number | Hits | Search Text  | DB              | Time stamp       |
|----------|------|--|-----------------|------------------|
| 1        | 180  | 438/24,46,69,82,48,99.ccls. and (source near3 electrode) and (drain near3 electrode)   | USPAT; US-PGPUB | 2004/10/28 12:58 |
| 2        | 121  | (438/24,46,69,82,48,99.ccls. and (source near3 electrode) and (drain near3 electrode) ) and @ad<20020711   | USPAT; US-PGPUB | 2004/10/28 12:58 |
| 3        | 1289 | 257/59,72,113,184,228,290.ccls. and (source near3 electrode) and (drain near3 electrode)   | USPAT; US-PGPUB | 2004/10/28 12:58 |
| 4        | 1061 | (257/59,72,113,184,228,290.ccls. and (source near3 electrode) and (drain near3 electrode) ) and @ad<20020711   | USPAT; US-PGPUB | 2004/10/28 12:58 |
| 5        | 1035 | ((257/59,72,113,184,228,290.ccls. and (source near3 electrode) and (drain near3 electrode) ) and @ad<20020711) not ((438/24,46,69,82,48,99.ccls. and (source near3 electrode) and (drain near3 electrode) ) and @ad<20020711)  | USPAT; US-PGPUB | 2004/10/28 12:59 |
| 6        | 1033 | ((257/59,72,113,184,228,290.ccls. and (source near3 electrode) and (drain near3 electrode) ) and @ad<20020711) not ((438/24,46,69,82,48,99.ccls. and (source near3 electrode) and (drain near3 electrode) ) and @ad<20020711)) and (gate)  | USPAT; US-PGPUB | 2004/10/28 12:59 |
| 8        | 874  | (((257/59,72,113,184,228,290.ccls. and (source near3 electrode) and (drain near3 electrode) ) and @ad<20020711) not ((438/24,46,69,82,48,99.ccls. and (source near3 electrode) and (drain near3 electrode) ) and @ad<20020711)) and (gate)) and (hole or trench or recess or aperture or via or opening) | USPAT; US-PGPUB | 2004/10/28 13:00 |

DOCUMENT-IDENTIFIER: US 20020158995 A1

TITLE: Polycrystalline silicon thin film  
transistor of liquid crystal display and manufacturing  
method thereof

----- KWIC -----

Summary of Invention Paragraph - BSTX (18) :

[0017] On the first and second contact holes 22a, 22b and the insulating interlayer 20 is deposited a metal layer. The metal layer is patterned using the photolithography process to thereby form a source/drain electrode 26a, 26b and a data line 16c (using the fifth mask).

Summary of Invention Paragraph - BSTX (19) :

[0018] Referring to FIG. 1B, on the source/drain electrode 26a, 26b, the data line 26c and the insulating interlayer 20, there is formed a passivation layer 28 made of the organic insulating material and the inorganic insulating layer. The passivation layer 28 is partially etched by the photolithography process to form a via hole 30 for exposing the source electrode 26a (using the sixth mask).

Summary of Invention Paragraph - BSTX (20) :

[0019] Then, after a transparent conductive layer or a reflective conductive layer is deposited on the via hole 30 and the passivation layer 28, the conductive layer is patterned by the photolithography process to form a pixel electrode 32 which is connected through the via hole 30 to the source electrode 26a (using a seventh mask).

Summary of Invention Paragraph - BSTX (36) :

[0034] According to the fourth embodiment of the present invention, after forming the data line, contact holes are formed at the same time. An electrode connected with the pixel electrode and the data line is formed from the same layer. That is, the image signal applied to the data line is transmitted to the drain region of the TFT through the drain electrode formed from the same layer as in the pixel electrode. Further, the pixel electrode is directly connected to the source region of a TFT without a separate source electrode.

Therefore, the number of used mask is reduced from 7 sheets to 6 sheets.

Detail Description Paragraph - DETX (50) :

[0095] On the data line 312 and the first insulating interlayer 310 is formed the second insulating interlayer 314 of the inorganic material such as SiO<sub>2</sub> and SiNx, or the acrylic photosensitive organic material. On the second insulating interlayer 314, there is formed a pixel electrode 318b which is directly connected with the source region 305S through the second contact hole 316b formed through the gate insulating layer 306, the first insulating interlayer 310 and the second insulating interlayer 314 on the source region 305S. On the second insulating interlayer 314, there is formed a drain electrode 318a which connects the data line 312 and the drain region 305D through the first contact hole 316a formed through the gate insulating layer 306, the first insulating interlayer 310 and the second insulating interlayer 314 on the drain region 305D and the third contact hole 316c formed at the second insulating interlayer 314 on the data line 312. The drain electrode 318a and the pixel electrode 318b are formed from the same

layer. When the positions of the source region 305S and the drain region 305D are exchanged each other, an electrode connected to the data line 312 is served as a source electrode. The pixel electrode 318b is directly connected to the drain region 305D.

Detail Description Paragraph - DETX (55) :

[0100] On the gate line, there is formed the data line 312 extending in the second direction (i.e., longitudinally) perpendicular to the first direction. The active pattern 304 is formed to be apart from the data line 312 at a desired interval. The gate electrode branched from the gate line 108 crosses the active pattern 104. A considerable portion of the capacitor line 308b is overlapped with a lower region (i.e., the source region) of the active pattern 304 crossed by the gate electrode. An upper region (i.e., the drain region) of the active pattern 104 crossed by the gate electrode is connected to the data line 312 by the drain electrode 316c. For this connection, the first contact hole 316a is formed at the drain region, and the third contact hole 316b is formed at a desired portion of the data line 312.

Detail Description Paragraph - DETX (56) :

[0101] The second contact hole 316b is formed at the drain region of the active pattern 304. The pixel electrode 316b formed from the same layer as in the drain electrode 316c is directly connected through the second contact hole 316b to the source region.

Detail Description Paragraph - DETX (70) :

[0115] Then, the conductive layer 318 is patterned using the photolithography process to form the drain electrode 318a

and the pixel electrode 318b (using the sixth mask), as shown in FIG. 9. The drain electrode

318a connects the drain region 305D and the data line 312 through the first contact hole 316a which is formed through the gate insulating layer 306, the first insulating interlayer 310 and the second insulating interlayer 314 on the drain region 305D and the third contact hole 316c which is formed through the second insulating interlayer 314 on an upper portion of the data line 312.

Detail Description Paragraph - DETX (88) :

[0131] Subsequently, although not shown in the drawings, the second photoresist pattern 320a is removed by an ashing and strip process. Afterwards, a conductive film is deposited on the contact holes 316a, 316b and 316c and the second insulating interlayer 316 and then patterned using a photolithography process to form a drain electrode 318a and a pixel electrode 318b as shown in FIG. 9.

Detail Description Paragraph - DETX (89) :

[0132] According to the first embodiment of the present invention, a data line and a pixel electrode capable of being made of the same material are formed from the same layer. Contact holes for respectively connecting the data line and the pixel electrode to a source region and a drain region of an active pattern are formed at the same time. That is, an image signal is transmitted to the drain region through the data line formed from the same layer as in the pixel electrode. Further, the pixel electrode is directly connected to the source region of a TFT without a separate source electrode. Therefore, the number of used mask is reduced from 7 sheets to 5 sheets, thereby simplifying a

manufacturing process.

Detail Description Paragraph - DETX (92) :

[0135] According to the fourth embodiment of the present invention, after forming the data line, contact holes are formed at the same time. An electrode connected with the pixel electrode and the data line is formed from the same layer. That is, the image signal applied to the data line is transmitted to the drain region of the TFT through the drain electrode formed from the same layer as in the pixel electrode. Further, the pixel electrode is directly connected to the source region of a TFT without a separate source electrode. Therefore, the number of used mask is reduced from 7 sheets to 6 sheets.